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	Filing Date		2004-02-24	
	First Named Inventor	Haw-minn Lu		
	Art Unit	2616		
	Examiner Name	Wellington Chin		
	Attorney Docket Number			

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	2	AGRAWAL, "Testing and Fault-Tolerance of Multistage Interconnection Networks," Computer, Apr. 1982, pp. 41-53, vol. 15, no. 4, IEEE, US	<input type="checkbox"/>
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	5	CHIN, et al., "Packet Switching Networks for Multiprocessors and Data Flow Computers," IEEE Transactions on Computers, Nov. 1984, pp. 991-1003, vol. 33, no. 11, IEEE, US	<input type="checkbox"/>
	6	KUMAR, et al., "Failure Dependent Performance Analysis of a Fault-Tolerant Multistage Interconnection Network," IEEE Transactions on Computers, Dec. 1989, pp. 1703-1713, vol. 38, no. 12, IEEE, US	<input type="checkbox"/>
	7	TZENG, et al., "Realizing Fault-Tolerant Interconnection Network via Chaining," IEEE Transactions on Computers, Apr. 1988, pp. 458-462, vol. 37. no. 4, IEEE, US	<input type="checkbox"/>
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☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

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A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Haw-minn Lu/	Date (YYYY-MM-DD)	2006-03-27
Name/Print	Haw-minn Lu	Registration Number	55407

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